Architecting a Multi-Voltage JTAG Chain

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As low-power, handheld devices become more prevalent, printed circuit boards with a mixture of 5-V, 3.3-V, 2.5-V, and 1.8-V devices have become common, making the design of a JTAG chain a challenging task. The designer must determine both the operating voltage of the JTAG chain and the order to place devices that operate at different voltages. This article, which compares several methods for designing a multi-voltage JTAG chain, provides some tips and techniques for making a robust, error-free design.

Daisy chaining, or connecting multiple DSPs, FPGAs, CPLDs, and other logic devices via their JTAG ports, allows them to be controlled using a single JTAG connector. Commonly applied on boards with multiple JTAG devices, daisy chaining connects the TDI and TDO pins to form a serial path. The input of the chain is TDI of the first device; the output of the chain is TDO of the last device. The TRST, TCK, and TMS pins of all devices are connected in parallel. The daisy chain can be designed to allow one or more devices in the chain to be bypassed for debugging purposes by providing jumpers that can be installed or removed depending on the desired target devices. The number of devices that can be daisy chained is theoretically unlimited, but timing problems and intermittent crashes frequently occur in chains having more than about eight devices, especially at higher clock rates.

To meet JTAG timing requirements, buffers should be placed on TCK and TMS to maintain signal integrity when more than about four devices are in the chain, and each buffer should drive no more than four devices. For example, a chain with six devices requires two buffers for TCK and two buffers for TMS. The driver should be high speed (low propagation delay), with enough strength to drive four or more devices.

A hardware engineer might need to daisy chain devices that do not have the same I/O voltages. Connecting all of the devices in a single chain may not be the best solution, so the designer should consider partitioning the chains in order to meet the requirements of proprietary debugging tools. Level translators may be needed to accommodate multiple voltage levels, and signal integrity must be maintained. Design and test complexity are significantly increased, and IEEE 1149.1 expertise is needed to integrate and test the system. Two methods for implementing multi-voltage JTAG chains are presented here.

Separate JTAG Chains for Each Voltage Family

This approach, recommended when multiple devices have the same I/O voltage, places all devices with the same JTAG I/O voltage in a single chain, using a separate chain for each voltage. Each chain supports all the devices in its category, eliminating the chance that other devices won't work properly, and reducing confusion when other vendors must interface with the JTAG chain. Figure 1 shows a JTAG chain with the same I/O voltage devices. No voltage translators (VT) are needed in this case.

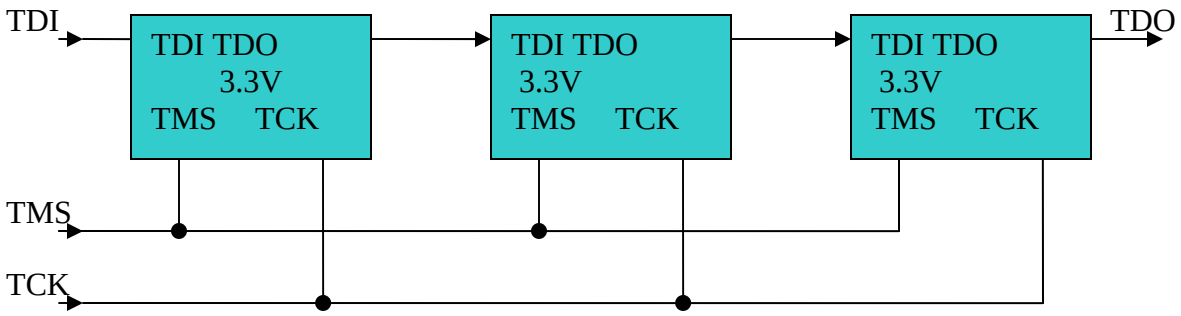

Figure 1: A JTAG chain with devices with the same I/O voltages

Multi-Voltage JTAG Chain

It is sometimes better to put all JTAG devices in a single chain. This approach is recommended when there are not enough devices in each voltage family to make a separate JTAG chain. The following requirements must be met to successfully interface two devices with different voltages in a JTAG chain:

VOHmin (minimum high output voltage) of the driver must be greater than VIHmin (minimum input high voltage) of the receiver.

VOLmax (maximum output low voltage) of the driver must be less than VILmax (maximum input low voltage) of the receiver.

The output voltage from the driver must not exceed the I/O voltage tolerance of the receiver.

Table 1 shows the common minimum and maximum voltages for different voltage standards. For more specific data, the designer should refer to the part's datasheet.

I/O STANDARD	V_{IL} (MIN)	V_{IL} (MAX)	V_{IH} (MIN)	V_{IH} (MAX)	V_{OL} (MAX)	V_{OH} (MIN)
LVTTL	-0.3	0.8	2.0	3.45	0.4	V_{CCO}-0.4
LVCMOS33	-0.3	0.8	2.0	3.45	0.4	V_{CCO}-0.4
LVCMOS25	-0.3	0.7	1.7	V_{CCO}+0.3	0.4	V_{CCO}-0.4
LVCMOS18	-0.3	35% V_{CCO}	65%V_{CCO}	V_{CCO}+0.3	0.45	V_{CCO}-0.45
LVCMOS15	-0.3	35% V_{CCO}	65%V_{CCO}	V_{CCO}+0.3	0.45	V_{CCO}-0.45

Table 1: Typical I/O standards and their associated Min and Max voltages.

Design Guidelines for a Multi-Voltage JTAG Chain

Place the highest voltage devices at the beginning of the chain, the next highest voltage next, and so on down to the lowest voltage devices being last. Placing the highest voltage to lowest voltage JTAG signals in order allows correct interpretation of a logic high on the TDO output of one device by the input of the next device.

Verify that each device is able to tolerate the maximum voltage from the proceeding device. For example if the first device is a 3.3-V part and the next one is a 1.8-V device, make sure that the 1.8-V part can tolerate at least 3.6 V on its inputs.

Verify that TDO coming from the lowest voltage device can be interpreted correctly by the emulator. In the example, make sure that the VOH_{min} of the 1.8-V device is greater than VIH_{min}

of the 3.3-V device. If not, a high-speed voltage translator should be used to translate TDO to the correct voltage for the emulator. The VT should not register (clock) the signal, as this will delay the signals for one clock, causing the JTAG chain to fail. The ADG3304 bidirectional logic level translator from Analog Devices contains four bidirectional channels that can be used in multi-voltage digital system applications. Figure 2 shows devices with 3.3-V, 2.5-V and 1.8-V I/O voltages where the device with the lower voltage has I/Os that can tolerate the higher voltage of the preceding device. A VT is used for TDO to pump up the voltage from 1.8 V to 3.3 V.

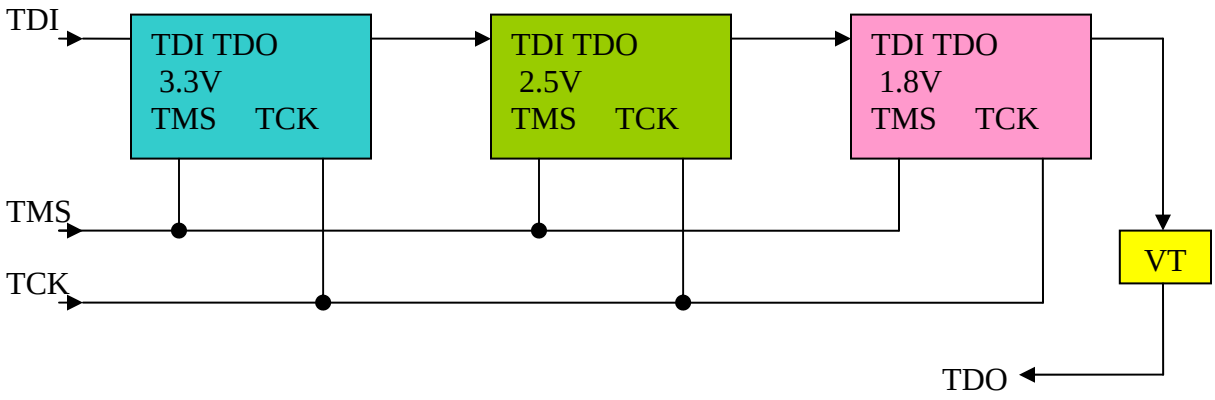

Figure 2: Three devices in a JTAG chain with different I/O voltages.

When a lower voltage device cannot tolerate the high voltage of the preceding device, a high-speed voltage translator should be used on all JTAG signals. The emulator should be used as the input to all voltage translators except for TDO. Don't cascade voltage translators, as this will increase the propagation delay. Figure 3 illustrates a case where the lower voltage part cannot tolerate the higher voltage I/O, so VTs are needed for each signal.

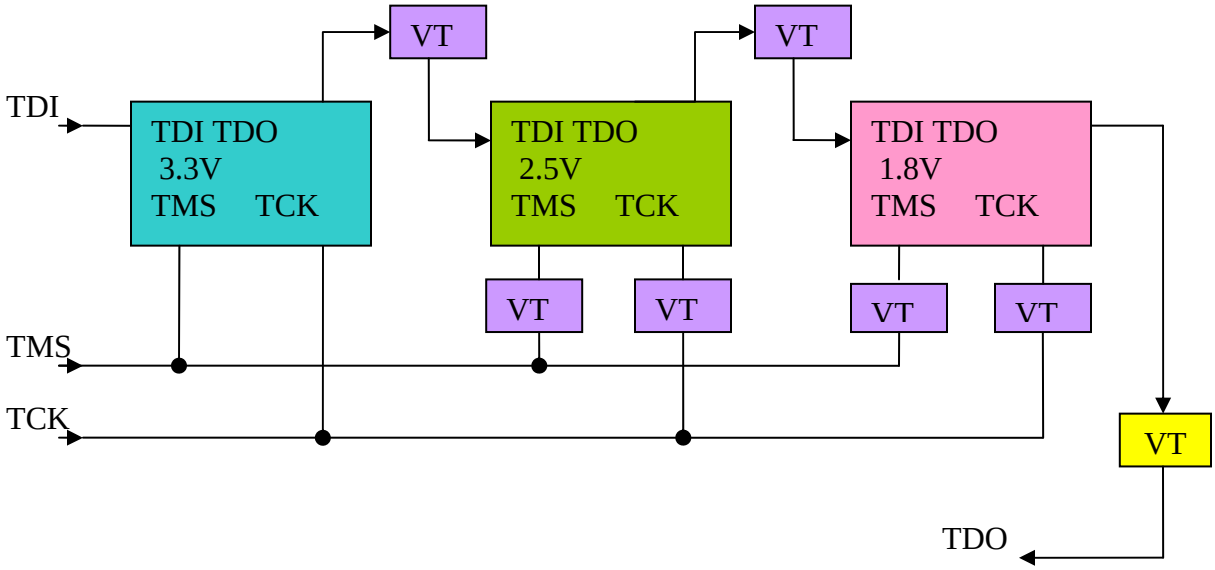

Figure 3: Three devices with different I/O voltages with voltage translators for JTAG signal.

If only a single device cannot tolerate the I/O voltages from the previous part, voltage translators are only required on that part. For example, with I/O voltages of 3.3 V, 2.5 V and 1.8 V in the

JTAG chain, the 1.8-V part has 2.5-V tolerant I/Os, so the 2.5-V signals can be used by the 1.8-V part. In Figure 4, the 2.5-V device does not have 3.3-V tolerant I/Os, but 1.8-V device is 2.5-V tolerant, so VTs are only used for the 2.5-V part.

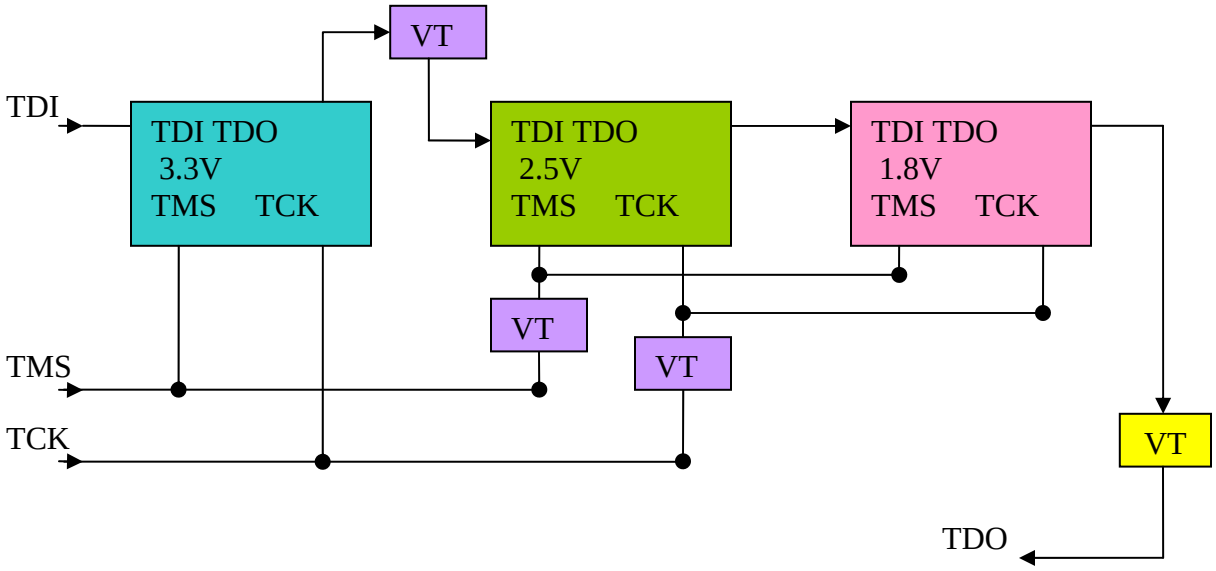

Figure 4: Three devices with different I/O voltages. The 1.8-V device has 2.5-V compatible I/Os.

Using a Schottky diode Instead of a Voltage Translator:
If a drop of about 0.4 V will suffice to adjust voltage levels from a higher voltage to a lower voltage level, a Schottky diode with fast recovery time can be used in place of the voltage translator. The 1SS383T1G Schottky diode from ON Semiconductor has a forward voltage drop of 0.48 V and a capacitive load of 25 pF. The SD103ATW from Diodes Inc., three fully isolated Schottky diodes with a forward drop voltage of about 0.3 V with a capacitive load of 50 pF may also be used in this application.

For complete details on JTAG signals, refer to "IEEE Standard Test Access Port and Boundary-Scan Architecture."